

**UNITED STATES PATENT APPLICATION**

**OF**

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**FOR**

**POLYSILICON THIN FILM TRANSISTOR**

**USED IN A LIQUID CRYSTAL DISPLAY**

**AND THE FABRICATING METHOD**

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a thin film transistor (TFT) of the type used in a liquid crystal display (LCD). More particularly, it relates to a polycrystalline silicon thin film transistor (Poly-Si TFT) and a method of manufacturing the same.

### Discussion of the Related Art

Generally, in order to form a polycrystalline silicon membrane, intrinsic amorphous silicon is first deposited by conventional methods, for example, Plasma Chemical Vapor Deposition (PCVD) or Low Pressure CVD (LPCVD). Then that amorphous silicon is 10 crystallized. The crystallization methods can be classified into three types.

Firstly, a metal induced crystallization (MIC) technique. The MIC technique can use large size glass substrates, since the MIC technique can use a low crystallization temperature.

Secondly, a solid phase crystallization (SPC) technique. SPC changes amorphous silicon into polycrystalline silicon by heat-treatment at a high temperature for a long time. It 15 requires forming a buffer layer on a quartz substrate in order to prevent the quartz substrate from diffusing an impurity material. The amorphous silicon layer is then deposited on the buffer layer and crystallized by the heat-treatment.

Thirdly, a laser annealing technique grows polycrystalline silicon using laser irradiation while heating a substrate having an amorphous silicon membrane.

20 Although metal induced crystallization (MIC) can form polycrystalline silicon on large sized glass substrates, the quality of the resulting membrane is questionable due to the high possibility of residual metallic material in the grain boundaries of the polycrystalline

silicon.

The solid phase crystallization (SPC) method results in irregular grain boundaries that cause the gate insulating layer on the polycrystalline silicon layer to grow erratically, leading to a low breakdown voltage. Furthermore, since the grain sizes of the polycrystalline silicon 5 are highly non-uniform, the electrical properties of the resulting device, such as the on-current and the threshold voltage, are not good. Finally, a costly quartz substrate should be employed when performing SPC.

The laser annealing technique is widely used and has been carefully investigated. This method can heat amorphous silicon on a glass substrate up to the melting temperature of the 10 silicon without damaging the substrate.

For a more complete understanding of laser annealing, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

Figs. 1a to 1d show the fabrication process steps of a TFT according to the related art. Referring to Fig. 1a, a first insulating layer 2 and an amorphous silicon layer 4 are 15 sequentially formed on a substrate 1. The first insulating layer 2 prevents the substrate 1 from effusing alkali. The first insulating layer 2 also acts as an antireflection layer the prevents leakage of the excimer-laser beam used in laser annealing.

Fig. 1b shows the process step of crystallizing the amorphous silicon layer 4. An excimer-laser beam quickly heats the amorphous silicon to its melting temperature. If the 20 excimer-laser irradiation stops, the amorphous silicon cools down quickly. Crystal growth of polycrystalline silicon then occurs with the numerous crystal nuclei acting as starting points or "seeds."

Referring to Fig. 1c, an island-shaped polycrystalline silicon 4 layer is formed by patterning the crystallized poly-silicon. A second insulating material and a first metallic material are deposited sequentially and patterned to form a second insulating layer 6 and a gate electrode 8. Then, the peripheral portion of the polycrystalline silicon 4 is ion-doped 5 using the gate electrode 8 as a mask.

As shown in Fig. 1d, a third insulating layer 11 is deposited and patterned to form contact holes on the doped portions 12 and 13. Then, source and drain electrodes 9 and 10 are formed in and around the contact holes.

However, the conventional laser annealing method uses the numerous crystal nuclei as 10 starting points (seeds) at random. The grain size of the polycrystalline silicon is then about 1  $\mu\text{m}$ . From these results, as shown in Fig. 2, many small-sized grains 20 are formed in the channel region of the TFT. This means that the grain boundaries, which affect the electrical properties, are numerous. This deteriorates the electrical properties of the TFT.

Referring to Fig. 3, the excimer-laser beam should be irradiated many times to obtain 15 a reliable TFT when large-sized amorphous silicon on a substrate 40 is being crystallized. To accomplish this a second excimer-laser beam 44 can be irradiated over about 90% of the area irradiated by the first excimer-laser. The amorphous silicon is then converted to polycrystalline silicon by repeating the overlap of the laser beams several times.

As the conventional method forms small-sized grains and numerous grain boundaries, 20 it does not produce good electrical properties when the length of TFT channel region is around 10  $\mu\text{m}$ .

To address these problems, Japanese Journal of Physics (JJAP), pp. 4545-4549, in

1992 and JJAP, pp. 70-74, in 1994 disclose TFTs having a gate electrode with a bridge structure. Figs. 4 and 5 explain those techniques.

An insulating layer 52 is formed on a silicon wafer 50, which has been constructed by removal of the central portion 50b of the silicon wafer 50 using preferential etching. Then, 5 amorphous silicon 54 is formed on the insulating layer 52. That silicon is then crystallized using an excimer-laser. The grain size of the polycrystalline silicon grows up to 50 $\mu$ m. In this method, the peripheral portion 50a of the silicon wafer 50 acts as the bridge, which supports the central portion 50b of the silicon wafer 50.

Fig. 5 shows a cross sectional view of a TFT that is made of polycrystalline silicon formed using that crystallization method (in Fig. 4). A gate electrode 56 is formed under the silicon wafer 52. Patterning yields the polycrystalline silicon active layer 54. After that, 10 source and drain electrodes 58 and 60 are formed.

The field-effect mobility of a TFT fabricated by the method of Figs. 4 and 5 is similar to that of a MOS (metal oxide silicon) transistor made of amorphous silicon.

15 These techniques, however, do not explain the method of forming the preferable grain size and shape. Furthermore, the method of fabricating plural uniform devices on a large size substrate is not suggested.

#### SUMMARY OF THE INVENTION

An object of the present invention is to provide a method of forming a polycrystalline 20 silicon layer having large-sized grains and a TFT fabricated by that method.

In order to achieve the object of the invention, the present invention provides a method of fabricating a thin film transistor (TFT), including: providing a substrate; depositing

amorphous silicon on the substrate; patterning the amorphous silicon to form plural island-shaped amorphous silicon layers, the amorphous silicon layers being parallel to each other; forming etched-spaces between the substrate and the amorphous silicon layers by etching the upper side of the substrate; forming ion stoppers on the corresponding island-shaped 5 amorphous silicon layers; defining channel regions and source and drain ohmic contact regions by doping ions on the island-shaped amorphous silicon layers using the ion stoppers as masks; removing the ion stoppers; forming a first insulating layer covering the amorphous silicon layer; crystallizing the amorphous silicon layers to form polysilicon layers by irradiating laser beams on the first insulating layer; forming a gate electrode on the first 10 insulating layer; forming a second insulating layer covering the gate electrode and the exposed polysilicon layers; patterning the second insulating layer to have contact holes to expose source and drain ohmic contact regions; and forming source and drain electrodes on the second insulating layer, the source and drain electrodes contacting the source and drain ohmic contact regions, respectively, via the contact holes.

15 In another aspect of the invention, the principles of the present invention provides a thin film transistor (TFT), including: a substrate; plural active layers above the substrate; spaces between the substrate and the plural active layers; a first insulating layer formed on the active layers; a gate electrode on the first insulating layer over the plural active layers; a second insulating layer covering the gate electrode and the active layers, the second insulating 20 layer having contact holes exposing both sides of the plural active layers; and source and drain electrodes on the second insulating layer while having electrical connection to the both sides of the active layers via the contact holes of the second insulating layer.

In another aspect, the principles of the present invention provides a thin film transistor (TFT), including: a substrate; plural active layers having cave-shaped-spaces between the active layers and the substrate, first-doped source and drain regions; silicon layers doped twice and having electrical connection with the first doped source and drain regions; a first insulating layer formed on the active layer; and a gate electrode formed on the first insulating layer.

5 In another aspect of the invention, the principles of the present invention provide a fabrication method of the thin film transistor (TFT), including: providing a substrate; depositing metallic material for a source and drain electrodes on the substrate; forming a space; forming a first amorphous silicon layer on the source and drain electrodes; forming a second amorphous silicon layer covering the first electrode and a substance; forming a first insulating layer on the second amorphous silicon layer; and forming gate electrode on the first insulating layer, corresponding to active layer.

10 In another aspect of the invention, the principles of the present invention provides a TFT, including: a substrate; plural active layers having a space between the substrate and the active layer; the first insulating layer covering the plural active layers; source and drain electrodes having the connection with the active layers; and a gate electrode corresponding to the active layers.

15 It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

### BRIEF DESCRIPTION OF THE DRAWING

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the 5 principles of the invention.

In the drawings:

Figs. 1a to 1d show cross sectional views illustrating the fabrication process steps of a TFT according to the related art;

Fig. 2 shows an enlarged plain view of a portion of a TFT according to related art;

10 Fig. 3 is a plan view illustrating a related art laser crystallization method;

Fig. 4 is a plan view illustrating the fabrication of a bridge structure in a related art;

Fig. 5 is a cross sectional view illustrating the bridge structure of a related art TFT;

Fig. 6 is a plan view illustrating a TFT according to a first embodiment of the present invention;

15 Figs. 7a to 7e are cross sectional views taken along line VII-VII of Fig. 6;

Fig. 8 shows the cross sectional view taken along line VIII-VIII of Fig. 6;

Figs. 9a and 9b show cross sectional views illustrating crystallization by a laser annealing technique;

20 Figs. 10a to 10e show cross sectional views illustrating the fabrication of a bridge structure;

Fig. 11 shows a plan view illustrating a TFT according to another embodiment of the invention;

Figs. 12a to 12e show cross sectional views taken along line XII-XII of Fig. 11;

Fig. 13 shows a cross sectional view taken along line XIII-XIII of Fig. 11;

Figs. 14a to 14d show cross sectional views illustrating a TFT according to another embodiment of the present invention; and

5 Fig. 15 shows a cross sectional view illustrating an array substrate for a LCD device according to the principles of the present invention.

#### DETAILED DESCRIPTION OF ILLUSTRATED EMBODIMENTS

Reference will now be made to embodiments of the present invention, examples of  
10 which are illustrated in the accompanying drawings.

Fig. 6 is a plan view illustrating a thin film transistor (TFT) according to a first embodiment of the invention. In particular, Fig. 6 shows a coplanar type TFT. That TFT has plural polycrystalline silicon layers 100, each of which includes a channel region 100c and source and drain ohmic contact regions 100a and 100b at the sides of the polycrystalline  
15 silicon layer 100. The source and drain ohmic contact regions 100a and 100b are doped by N-type or P-type ions. A gate electrode 108 is formed adjacent the channel regions 100c. Source and drain electrodes 106 and 104, positioned on the sides of the gate electrode 108, have electrical connections to the source and drain ohmic contact regions 100a and 100b via contact holes.

20 The illustrated embodiment TFT has plural active layers 100 and plural channel regions 100c. The plural channel regions 100c are connected in parallel. That improves the electrical characteristics of the composite channel region.

Figs. 7a to 7e are cross sectional views taken along line VII-VII of Fig. 6, and thus show only one of the paralleled active layers.

Referring to Fig. 7a, amorphous silicon is deposited on a substrate 1 and then patterned in the shape of an island to form an active layer 100.

5 Fig. 7b shows ion doping of the amorphous silicon layer 100. Before doping an ion stopper 110 is formed on the amorphous silicon layer 100 above where a channel region 100c is to be located. The ion stopper 110 can be an organic photoresist layer or an inorganic insulating layer. Thus, the amorphous silicon layer 100 is doped, except at the channel region.

The characteristics of the TFT can be varied by the gas used during the doping process. For example, using  $H_2B_6$ , which includes a group III element, defines a P-type TFT while using  $PH_3$ , which includes a group V, element defines an N-type TFT.

A space 116 between the amorphous silicon layer 100 and the substrate 1 is created by etching the upper side of the substrate 1. To etch the upper side of the substrate 1, a buffered-HF solution having a very high etch rate is employed.

15 Fig. 7c illustrates the crystallization process of the amorphous silicon 100. A first insulating layer 118 is formed over the amorphous silicon layer 100. Then, laser beams irradiate the first insulating layer 118 such that the amorphous silicon layer 100 is crystallized by laser annealing. The insulating layer acts as an antireflection layer.

Referring to Fig. 7d, a gate electrode 108 is then formed by deposition and patterning. 20 When patterning, the first insulating layer 118 and the gate electrode 108 can be patterned at the same time or individually. The patterned first insulating layer 118 acts as a gate insulating layer. After that, a second insulating layer 124 is formed over the gate electrode 108 and the

source and drain ohmic contact regions 100b and 100a. The second insulating layer 124 is then patterned to form contact holes 102 that expose the source and drain ohmic contact regions 100b and 100a.

As shown in Fig. 7c, source and drain electrodes 106 and 104 are formed on the 5 second insulating layer such that they have electrical connections to the source and drain ohmic contact regions 100b and 100a, respectively, through the contact holes 102.

Fig. 8 shows a cross sectional view taken along line VIII-VIII of Fig. 6. The substrate 1 has etched-spaces 116 that are bridged by the plural polycrystalline active layers 100. The first insulating layer 118 (which act as gate insulators) is over the active layer 100 and 10 substrate, filling in the remaining portions of the etched-parts of the substrate 1. The gate electrode 108 and the second insulating layer 124 are formed on the first insulating layer 118.

Figs. 9a and 9b show cross sectional views illustrating the function of the etched-spaces 116 during laser annealing crystallization. The laser crystallization process begins by irradiating laser beams on the substrate 1 and on the amorphous silicon layer 100. The density 15 of the laser energy should be enough to melt the amorphous silicon. When laser irradiation stops, the amorphous silicon layer cools down almost immediately and becomes polycrystalline silicon. Beneficially, the density of the laser energy preferably ranges between 200 and 250 mJ/cm<sup>2</sup>.

As shown in Fig. 9a, the cooling of the melted amorphous silicon layer 100 is not 20 uniform. In the "A" of the active layer 100, which corresponds to the section over the etched-space 116, cooling is relatively slow, while in area "B", which corresponds to the section on the substrate, cooling is relatively fast. The difference in solidification rates is due to the

etched-spaces 116 having a lower thermal conductivity than the substrate. Latent heat produced by laser irradiation in area "B" is diffused into the substrate 1. Thus, the molten silicon starts to solidify relatively rapidly at the interface between the silicon and the substrate. On the other hand, the latent heat in area "A" is not diffused as much. Thus, the 5 molten silicon begins solidifying from the edge and remains in a liquid state for a relatively long time over the etched-space 116.

Referring to Fig. 9b, the cooling starting points or "seeds" are generated at random in the area "B". Uniform grains occur from the numerous crystal nuclei that become the starting points or "seeds". Grain growth ceases when the grain boundaries come in contact with each 10 other. However, the silicon in area "A" remains in a liquid state for a relatively long time.

Due to the fact that seeds "S" are created in area "B", a lateral growth of the seeds from area "B" into the area "A" occurs. Furthermore, the vertical growth ceases around the center of the thickness "W". Owing to this phenomena, the slower solidification rate and the lateral growth of grains are very effective in enlarging the grains in area "A". The grain size in area "A" 15 depends on the thermal storage capacity of the etched-space 116. This can be controlled by the shape and the size of the etched-space 116.

When the polycrystalline silicon produced by the foregoing method is used to make a TFT, due to the fact that such a thin-film transistor (TFT) has an active layer 100 with large grains and fewer grain boundaries, the characteristics of the thin-film transistor are improved.

20 As shown in Figs. 9a and 9b, the lateral growth velocity of the grains depends on the length " $\Delta L$ " of the source and drain ohmic contact regions 100a and 100b. As that length becomes longer, the growth velocity becomes less during the crystallization process. When

the length "L" of the channel region 100c and the thickness "W" of the active layer 100 are reduced in the fixed area "A", the total area of the grain boundaries is reduced.

To obtain the best results, which can be comparable to those of a mono-crystal grain (which is ideal), the lengths " $\Delta L$ " and "L" and the thickness "W" should be optimized. In 5 one embodiment, the preferred values are about 5 $\mu\text{m}$  for the length " $\Delta L$ ", about 6 $\mu\text{m}$  for the length "L" and about 5 $\mu\text{m}$  for the thickness "W".

Another aspect of the invention relates to methods of forming spaces between the substrate and the plural active layers. While etching the substrate, to prevent the polycrystalline silicon from developing internal stresses or cracks, a bridge structure having 10 an arch shape and piers can be used.

Figs. 10a and 10b are cross sectional views illustrating a method of forming spaces by etching the upper part of the substrate, while Figs. 10c to 10e are cross sectional views illustrating a method of forming spaces by etching a layer interposed between the substrate and the active layers.

15 Fig. 10a, which is similar to Fig. 7c, shows a cross sectional views illustrating a method of forming piers 132. Plural amorphous silicon layers 100 are formed on a substrate 1. Etching the upper side of the substrate 1 forms the spaces 116 between the substrate 1 and the amorphous silicon layers 100. While etching the substrate 1, a plurality of non-etched portions or piers 132 are formed to support the amorphous silicon layer 100. The etching 20 process may include a masking process for blocking the portions where the piers 132 are formed. The structure of the piers 132 prevents the amorphous silicon layer 100 from physical strain such as longitudinal stress or axial stress. The electrodes 104 and 106, formed before

forming the active layer 100, can serve as source and drain electrodes for a TFT. Fig. 10b, which is similar to Fig. 10a, illustrates a method of forming auxiliary piers 133. When forming the electrodes 104 and 106, the auxiliary piers 133 are also formed on the substrate 1. Then, the amorphous silicon 100 is deposited on the substrate 1 and on the auxiliary piers 5 133. After that, the spaces 116 are formed by etching the substrate 1.

As shown in Fig. 10c, a forming-space substance 115, such as silicon oxide ( $\text{SiO}_2$ ) or Chrome, is deposited on the substrate 1. Then the amorphous silicon layer 100 is subsequently formed. The amorphous silicon layer 100 is formed into an island shape by patterning. Then the substance 115 is selectively etched using a mask technique to form the 10 spaces 116 and to leave non-etched portions 134, which serve as piers or supporters for the active layers 100.

Referring to Fig. 10d, a metallic material is first deposited on the substrate 1. Then, source and drain electrodes 106 and 104 are formed by patterning the metallic material. The patterned metallic material includes not only source and drain portions 106 and 104, but also 15 portions for piers 134 and portions corresponding to the spaces 116. Thus, during patterning, a pluralities of piers 134 are formed simultaneously. The amorphous silicon layer 100 is then formed on the patterned metallic material. Then, the portions of the metallic material corresponding to the spaces 116 are etched and removed using a mask. Therefore, the remaining portions of the metallic material are piers 134 and source and drain electrodes 106 20 and 104. The number of the piers 134 can be more than two.

Fig. 10e shows a cross sectional view illustrating a method of forming a space 116 having no piers 134. The source and drain electrodes 106 and 104 are first formed on the

substrate 1. Then, the metallic material for the space 116 is formed between source and drain electrodes 106 and 104. After that, an amorphous silicon layer 100 that covers the source and drain electrodes and the metallic material is formed. The space 116 is then formed by removing the metallic material. In this embodiment, the border "H" between the source and drain electrodes and the cave-shaped-space 116 indicates a bridge structure having an arch shape. Silicon oxide ( $\text{SiO}_2$ ) can be used to form the space 116 instead of a metallic material.

Fig. 11 shows a plan view illustrating a poly-silicon TFT made using a method according to Figs 10a to 10e. Moreover, Fig. 11 shows a staggered type TFT. The TFT has plural polycrystalline silicon layers 100, each of which include a channel region 100c and source and drain ohmic contact regions 100a and 100b on the sides of the polycrystalline silicon layers 100. The source and drain ohmic contact regions 100b and 100a are doped by impurity ions. A gate electrode 108 is formed adjacent the channel regions 100c. Source and drain electrodes 106 and 104, positioned on the sides of the gate electrode 108, have electrical connections to the source and drain ohmic contact regions 100b and 100a.

Figs. 12a to 12e illustrate a fabrication process along line XII-XII of Fig. 11. Referring to Fig. 12a, source and drain electrodes are formed on the substrate 1. Then, a space-forming substance 150 is deposited over the source and drain electrodes 106 and 104 and over the substrate 1. The space-forming substance 150 is beneficially made of silicon oxide ( $\text{SiO}_2$ ) or silicon nitride ( $\text{SiN}_x$ ). It could also be made of metallic material selected from a group consisting of Molybdenum, Chrome, Aluminum, Titanium, Tantalum, etc., which can also be the material for the source and drain electrodes.

As shown in Fig. 12b, the space-forming substance 150 is patterned in an island shape

152 that is spaced apart from the source and drain electrodes 106 and 104. An amorphous silicon layer 100 then covers the island shape 152 and part of the source and drain electrodes.

Referring to Fig. 12c, a space 116 is then formed by etching the island shape 152.

Then, an ion stopper 110 is formed on the amorphous silicon layer 100 over the space 116.

5 Then an ion-doping process is used on the active layer 100 to produce a channel region 100c and source and drain ohmic contact regions 100b and 100a, see Fig. 12d. The ion stopper acts as a mask. After stripping the ion stopper 110 off, a first insulating layer 120 is formed on the amorphous silicon layer 100. Then laser crystallization is performed. During crystallization, a lateral growth from the sides of the space 116 occurs (see Figs. 9a and 9b).

10 Thus the fabrication of the TFT is completed, as shown in Fig. 12e. After forming a gate electrode 108 on the gate insulating layer 120 and forming a second insulating layer 154 the fabrication of the TFT is complete.

Fig. 13 shows a cross sectional view taken along line XIII-XIII of Fig. 11. The plurality of active layers 100 are connected in parallel. The first insulating layer 120 fills 15 between the spaces 116. The gate electrode 108 is formed on the first insulating layer 120 and then the second insulating layer 154 is formed on the gate electrode 108.

The principles of the present invention can fabricate a TFT having a LDD (lightly doped drain) structure. The LDD structure is applied to a MOS (metal oxide silicon) transistor, to protect the drain ohmic contact region from deterioration caused by hot carriers.

20 This method uses different ion densities to decrease deterioration caused by hot carriers. Thus, the ion doping process for the LDD-TFT is performed twice.

Referring to Fig. 14a, source and drain electrodes 106 and 104 are formed on the

substrate 1. Then a space-forming substance 152 is formed between the source and drain electrodes 106 and 104. An island-shaped amorphous silicon layer 160a is then formed on the source electrode and on the drain electrodes. Then a first doping process is then performed.

As shown in Fig. 14b, an amorphous silicon layer 100 that covers the space-forming substance 152 and part of the source and gate electrodes and their island-shaped amorphous silicon layers 160a is formed. Then, on the amorphous silicon layer 100 an ion stopper 110 is formed over to the space-forming substance 152. Subsequently, the second ion doping process is performed. The space 116 is then created by etching the space-forming substance 152. Moreover, the ion stopper 110 is removed.

Owing to these processes, a difference between the first doping density and second doping density is created. Let us suppose that the first doping density is "N" and the second doping density is "M". The island-shaped silicon layer 160a (in Fig. 14a) has the ion density "N" while the island-shaped silicon layer 160b (in Fig. 14b) has the ion density "N+M". Moreover, the source and drain regions 161 adjacent the amorphous silicon layer 100 has the ion density "M". Thus, a channel region 100c and source and drain regions 161 are defined by the second doping ions using the ion stopper 110 as a mask.

Referring to Fig. 14c, a first insulating layer 120 that covers the island-shaped silicon layer 160c and the amorphous silicon layer 100 is formed. Then a laser crystallization process is performed. Thus, a channel region 100c and source and drain ohmic contact regions 160c are produced.

The source and drain regions 161 and the ohmic contact regions 160c have the same general electrical characteristics, but have different doping density levels.

As shown in Fig. 14d, a gate electrode 108 is then formed on the first insulating layer 120, and then a second insulating layer 154 is formed on the gate electrode 108. Contact holes that penetrate the first and second insulating layers are formed to expose the surface of the source and drain ohmic contact regions 160c. Finally, source and drain outer electrodes 162 and 164 that electrically connect to the ohmic contact regions 160c are formed.

5 An array substrate TFT for a LCD device having driving circuits fabricated using the above explained methods for forming polysilicon layer also can be produced.

The LCD device consists of an LC panel and external drive circuits. Technique for connecting the external drive circuits to the LC panel includes WB (wire bonding), COB 10 (chip on board), TAB (tape automated bonding), and COG (chip on glass) bonding.

Nowadays, lap top computers include pixel arrays made of amorphous silicon and drive 15 circuits made of mono-crystal silicon. However, because of the techniques of polysilicon crystallization described above, it is possible to fabricate TFTs of an LC panel and its drive circuits together. This is possible because the foregoing techniques of producing TFTs results in such large-sized-grain polycrystalline silicon that the polycrystalline silicon can have electrical characteristics comparable to mono-crystal silicon, thus leading to lower production costs.

Fig. 15 shows a cross sectional view of an array substrate having drive circuits for a LCD device. The CMOS drive circuit 228(Complementary metal oxide silicon) is comprised 20 of an N-type TFT 204 and a P-type TFT 206. The pixel 202 and the switching TFT 200 are located on the same substrate. The CMOS drive circuit 228 has a connection with the gate and source electrodes 108 and 210 of the switching TFT 200 and thus controls the switching

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TFT 200. The fabrication method for the TFT 200 and the CMOS 228 is as described above.

Thus, an additional description is not required.

As described above, according to the principles of the present invention, a TFT has a parallel connection of plural channel regions to improve its electrical characteristics. A space 5 between the substrate and the active layer aids forming large grains for the polycrystalline silicon layer of the TFT. Furthermore, such fabrication techniques can be used to form a LCD device having switching TFTs, and pixel and drive circuit fabricated as one body.

It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the 10 invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.